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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,724	02/10/2004	Masatoshi Yasutake	S004-5210	3824

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ADAMS & WILKS
31st Floor
50 Broadway
New York, NY 10004

EXAMINER	
JEFFERSON, QUOVAUNDA	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 11/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/775,724	YASUTAKE ET AL.	
	Examiner	Art Unit	
	Quovaunda Jefferson	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) *17-35* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Claims 17-35 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on October 19, 2005.

Applicant's election of claims 1-16 in the reply filed on October 19, 2005 is acknowledged. The applicant did not distinctly and specifically point out the supposed errors in the restriction requirement. Since the applicant did not clearly distinguish the lack of distinction between the different inventions, namely Group I, claims 1-16 and Group II, claims 17-35, there is no traversal in the election of Group I claims. The election is considered as an election without traverse and therefore Group II claims are cancelled (MPEP § 818.03(a)).

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

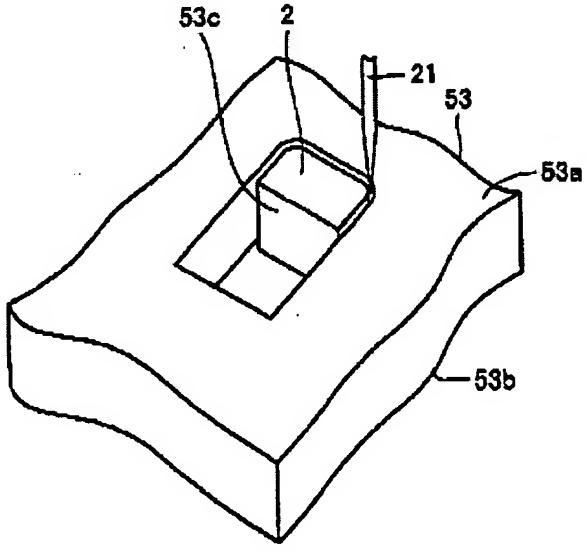
Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3 are rejected under 35 U.S.C. 102(e) as being anticipated Hirose, US Patent 6,826,971

FIG.7



Regarding claim 1, Hirose teaches a method of preparing a sample chip and observing its wall surface, comprising:

a first step including irradiating a sample with a focused energy beam, etching a surrounding area and a bottom portion of a predetermined area, and making the sample chip, (column 4, lines 62 and 63),

a second step of taking out the sample chip from the sample (column 5, lines 18 and 19),

and a third step of observing a wall surface of the taken sample chip with a scanning probe microscope (SPM) (column 7, line 55).

Regarding claim 2, Hirose teaches the method of preparing a sample chip and observing its wall surface of claim 1, wherein said focused energy beam is a focused ion beam (column 4, lines 62 and 63).

Regarding claim 3, Hirose teaches the method of preparing a sample chip and observing its wall surface of claim 2, wherein said first step includes processing the sample chip so that a stepped portion according surface to difference in material is formed in a surface to be observed with the scanning probe microscope (Figure 7).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4-6, 10, 12, 13, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirose as applied to claims 1-3 above, and further in view of Hirose et al, US Patent 5,783,830.

Regarding claim 4, Hirose teaches a method of preparing a sample chip and observing its wall surface, comprising of a first step including irradiating a sample with a focused energy beam, etching a surrounding area and a bottom portion of a predetermined area, and making the sample chip (column 4, line 62 and 63), a second step of taking out the sample chip from the sample (column 5, line 18 and 19), and a third step of observing a wall surface of the taken sample chip with a scanning probe microscope (column 7, line 55)

Hirose fails to teach a fourth step of irradiating the SPM-observed surface of the taken sample chip with the focused energy beam thereby to etch the SPM-observed surface and a step of repeating said third and fourth steps only a required number of times again. Hirose et al teaches a fourth step of irradiating the SPM-observed surface of the taken sample chip with the focused energy beam thereby to etch the SPM-observed surface and a step of repeating said third and fourth steps only a required

number of times again (column 4, lines 10-16). It would have been obvious to one skilled in the art to combine the teachings of Hirose et al with that of Hirose because if the observation point cannot be clearly observed, the sample is returned to the focus ion beam for its additional processing (Hirose et al, column 4, lines 10-13)

Regarding claim 5, Hirose further teaches the method of preparing a sample chip and observing its wall surface of claim 4, wherein said focused energy beam is a focused ion beam (column 4, lines 62 and 63).

Regarding claim 6, Hirose further teaches the method of preparing a sample chip and observing its wall surface of claim 5, wherein said first step includes processing the sample chip so that a stepped portion according to difference in material is formed in a face to be observed with the scanning probe microscope (Figure 7).

Regarding claim 10, Hirose teaches a method of preparing a sample chip and observing its wall surface, comprising of a first step including irradiating a sample with a first focused energy beam, etching a surrounding area and a bottom portion of a predetermined area, and making the sample chip (column 4, line 62 and 63) and a second step of taking out the sample chip from the sample. Hirose fails to teach teaches a third step of irradiating a specified wall surface, which the SPM-observed surface of the taken sample chip makes, with a second focused energy beam thereby to etch the wall surface, a fourth step of observing the wall surface of the sample chip, which has

undergone the etching by the second focused energy beam in said third step, a fifth step of irradiating the SPM-observed surface of the taken sample chip with the first focused energy beam thereby to etch the SPM-observed surface and a step of repeating said third to fifth steps only a required number of times again.

Hirose et al teaches a third step of irradiating a specified wall surface, which the SPM-observed surface of the taken sample chip makes, with a second focused energy beam thereby to etch the wall surface, a fourth step of observing the wall surface of the sample chip, which has undergone the etching by the second focused energy beam in said third step, a fifth step of irradiating the SPM-observed surface of the taken sample chip with the first focused energy beam thereby to etch the SPM-observed surface and a step of repeating said third to fifth steps only a required number of times again (columns 3 and 4).

Regarding claim 12, Hirose further teaches the method of preparing a sample chip and observing its wall surface of claim 11, wherein said first step and/or fifth step include processing the sample chip so that a stepped portion according to difference in material is formed in a face to be observed with the scanning probe microscope (Figure 7).

Regarding claim 13, Hirose teaches a method of preparing a, sample chip and observing its wall surface, comprising of a first step including irradiating a sample with a first focused energy beam, etching a surrounding area and a bottom portion of a

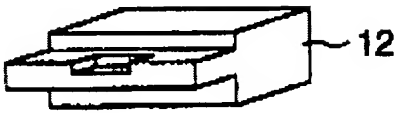
predetermined area, and making the sample chip (column 4, lines 62 and 63) and a second step of taking out the sample chip from the sample (column 5, lines 18 and 19). Hirose fails to teach a third step of irradiating a specified wall surface, which the SPM-observed surface of the taken sample chip makes, with a second focused energy beam thereby to etch the wall surface, a fourth step of observing the wall surface of the sample chip, which has undergone the etching by the second focused energy beam in said third step, a fifth step of irradiating the SPM-observed -surface of the taken sample chip with the second focused energy beam thereby to etch the SPM-observed surface, and a step of repeating said fourth and fifth steps only a required number of times again.

Hirose et al teaches a third step of irradiating a specified wall surface, which the SPM-observed surface of the taken sample chip makes, with a second focused energy beam thereby to etch the wall surface, a fourth step of observing the wall surface of the sample chip, which has undergone the etching by the second focused energy beam in said third step, a fifth step of irradiating the SPM-observed -surface of the taken sample chip with the second focused energy beam thereby to etch the SPM-observed surface, and a step of repeating said fourth and fifth steps only a required number of times again (columns 3 and 4).

Regarding claim 15, Hirose further teaches the method of preparing a sample chip and observing its wall surface of claim 14, wherein said first step includes processing the sample chip so that a stepped portion according to difference in material

is formed in a observed surface to be observed with the scanning probe-microscope (Figure 7).

FIG.5A



Regarding claim 16, Hirose et al teaches the method of preparing a sample chip and observing its wall surface of claim 1 wherein the sample chip to be cut off is shaped into an asymmetric form thereby to allow the observed surface of the sample chip for observation with the scanning probe microscope to be identified (Figure 5A).

Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirose as applied to claims 1-3 above, and further in view of Mizumura et al, US Patent 5,825,035.

Regarding claim 7, Hirose teaches a method of preparing a sample chip and observing its wall surface, comprising of a first step including irradiating a sample with a first focused energy beam, etching a surrounding area and a bottom portion of a

predetermined area, and making the sample chip (column 4, lines 62 and 63) and a second step of taking out the sample chip from the sample (column 5, lines 18 and 19),

Hirose fails to teach a third step of irradiating a specified wall surface, which the SPM-observed surface of the taken sample chip makes, with a second focused energy beam thereby to etch the wall surface and a fourth step of observing the wall surface of the sample chip, which has undergone the etching by the second focused energy beam in said third step. Mizumura teaches a third step of irradiating a specified wall surface, which the SPM-observed surface of the taken sample chip makes, with a second focused energy beam thereby to etch the wall surface (column 27, lines 42-50) and a fourth step of observing the wall surface of the sample chip, which has undergone the etching by the second focused energy beam in said third step (column 28). It would have been obvious to one skilled in this art to combine the teachings of Mizumura with that of Hirose because etching can be done and not influence the electrical characteristics of a sample to be processed (Mizumura, column 7, line 56 and 57).

Regarding claim 8, Mizumura further teaches the method of preparing a sample chip and observing its wall surface of claim 7, wherein said first focused energy beam is a focused ion beam, and said second focused energy beam is an argon ion beam (column 27).

Regarding claim 9, Hirose further teaches the method of preparing a sample chip and observing its wall surface of claim 8, wherein said first step includes processing the

sample chip so that a stepped portion according to difference in material is formed in a face to be observed with the scanning probe microscope (Figure 7).

Claims 11 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirose and Hirose et al as applied to claim 10 above, and further in view of Mizumura et al, US Patent 5,825,035.

Regarding claim 11, Hirose and Hirose et al fail to teach the method of preparing a. sample chip and observing its wall surface of claim 10, wherein said first focused energy beam is a focused ion beam, and said second focused energy beam is an argon ion beam. Mizumura teaches the method of preparing a. sample chip and observing its wall surface of claim 10, wherein said first focused energy beam is a focused ion beam, and said second focused energy beam is an argon ion beam (column 27). It would have been obvious to one skilled in this art to combine the teachings of Mizumura with that of Hirose and Hirose et al because etching can be done and not influence the electrical characteristics of a sample to be processed (Mizumura, column 7, line 56 and 57).

Regarding claim 14, Mizumura teaches the method of preparing a sample chip and observing its wall surface of claim 13, wherein said first focused energy beam is a focused ion beam, and said second focused energy beam is an argon ion beam (column 27).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US Patent 6,838,685, issued to Kodama et al, discloses an ion beam apparatus and ion beam processing method. US Patent Application Publication, by Tokuda et al, discloses a method and apparatus for processing a microsample.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quovaunda Jefferson whose telephone number is 571-272-5051. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

qvj

W. David Coleman
Primary Examiner